Simplifying FPGA Complexity

CAMPERA electronic systems

CES Utility Library Facts

ASIP

The UTILITY LIBRARY is a collection of modules that are used in almost every FPGA design. All the modules are vendor independent high quality VHDL code, with self checking testbenches and documentation.

In the UTILITY LIBRARY Customers will find a full set of memory modules (single port, dual port, true dual port), synchronous and asynchronous FIFOs, Encoders and Decoders and a lot of other essential modules.

Key Features

- vendor independent "off the shelf" VHDL cores for FPGAs (Xilinx, Altera, Achronix, Lattice and Microsemi)
- VHDL modules are written in pure VHDL-93 standard (2008 available on demand), completely vendor independent
- optimized in terms of speed, power and resource usage
- architected, developed, verified, released and maintained through a rigorous and efficient process
- DO-254 and IEC-61508 compliance if required

Key Benefits

- No cost for hardware/tool version update/upgrade
- No time to re-generate the cores for different targets and/or tools
- Considerably faster simulations compared to vendor pre-synthesized IP Cores
- Configurable high quality VHDL modules available at no cost
- Customization available on demand
- More than 150 useful functions in the ces_util package
- More than 13.000 lines of VHDL source code and 7000 lines of comments
- CES internal VHDL coding standard to help you quickly understand the source code
- The ces_util_lib is the swiss army knife of every FPGA designer and is ideal for expert designers as well as beginners
- Ideal for Companies who start to work on FPGA design to start designing with a complete library of modules and to see how a professional VHDL project and source code shall be.

Applications

- All FPGA\CPLD design

Deliverables

- VHDL source code
- Full set of documentation

Who we are

Campera Electronic Systems (CES) is a high technology, privately held, startup based in Livorno, Italy, with more than 10 years of experience on high performance FPGA design and Digital Signal Processing.
Established in March 2014 has grown rapidly with a focus on FPGA and its applications. The Company has developed proprietary HDL Design Flow, techniques and utilities and an immense HDL IP cores library, with fully verified high performance building blocks.

Benefits of libraries

VHDL libraries are a powerful mechanism the language offers to collect common modules together for reuse. Reuse is a key to success with FPGA design, it helps to design faster, easier and with verified and validated modules. Designing and testing a general purpose library is often considered as a time consuming effort and most often there is no time for FPGA designers to build a complete general purpose library.
Using our library allow designers to focus on high-level design without wasting time to develop building blocks.

Quality and support

Campera Electronic Systems works to the highest quality standards and developed a rigorous design flow that dramatically reduce design flaws at each stage of the development process.
Customers with a valid support contract can benefit from our 24/7 support by mail and phone, all optional modules, testbenches and more.

Contacts

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CES Utility Library: list of IP cores

CES UTILITY LIBRARY MODULES

Module name	*Description*
ces_util_ccd_switch	Cross clock domain switch
ces_util_counter	General purpose configurable counter. Can be used also as Watchdog timer
ces_util_mux	General purpose multiplexer
ces_util_demux	General purpose demultiplexer
ces_util_delay	Delay with architecture SRL, memory or pulse
ces_util_delay_var	Variable delay module with SRL, memory or pulse architecture
ces_util_encoder	General purpose encoder
ces_util_file_read/write	Read or write formatted signals on files, for simulation purposes
ces_util_clock_gen	Single ended or differential clock generator for simulation purposes
ces_util_pkg	Utility package with more than 150 useful functions
ces_util_sync_pulse	Synchronize a pulse through a cross clock domain
ces_util_ram_crw_crw	Synthesizable ram modules, single, simple dual, true dual port. The memory content can be initialized from an external text file
ces_util_fifo_sync	Synchronous FIFO, with configurable depth and width
ces_util_fifo_async	Asynchronous FIFO with two clock domains

Each VHDL module in the Utility Library can be easily configured via generics, reset type (sync or async), reset level (active low or active high), output value on reset, memory depth and data width, to mention a few.
To allow for proper instantiation of hard core modules (such as Block Ram or DSP) a generic with vendor, synthesis tool and other specific information is propagated to each module.

CES UTILITY LIBRARY OPTIONAL

Customization	Customers can add specific features or functionalities to each module on demand
Safety Critical book	Verification and validation reports for safety critical applications (DO-254 and EC-61508) can be provided on demand.
AXI wrapper option	AXI4, AXI4 Stream and AXI4 Lite wrapper can be supplied on demand
VHDL 2008 version	Customers using VHDL 2008 can benefit of the readability and other improvements introduced with VHDL 2008. All the Utility modules have a corresponding VHDL 2008 version which can be supplied on demand

Tested on Hardware: YES	**Deliverables**	**Supported FPGAs**
Verification and Validation (opt)	VHDL Source Code Documentation	Any
Self checking test bench Static timing analysis Code coverage Linting		**Supported Simulators** Active-HDL v9.1 or higher and Riviera Pro v2014.02 or higher **Supported Synthesizers** Mentor Precision r2013b.15 or later, Xilinx ISE 14.7/Vivado 2013.4 or later, Quartus II v.14 or later