Simplifying FPGA Complexity

CAMPERA electronic systems

CES Math Library Facts

ASIP

The MATH LIBRARY is a collection of modules that are used in almost every FPGA design. All the modules are vendor independent high quality VHDL code, with self checking testbenches and documentation.

In the MATH LIBRARY Customers will find a full set of mathematical VHDL modules for integer, fixed point and floating point (single or double precision, IEEE-Standard-754 compliant) arithmetic. Both real and complex data types are supported. Trigonometric function are implemented.

Key Features

- vendor independent "off the shelf" ASIP cores for FPGAs (Xilinx, Altera, Achronix, Lattice and Microsemi)
- ASIPs are written in pure VHDL (in 93 or 2008 version), completely vendor independent
- optimized in terms of speed, power and resource usage
- architected, developed, verified, released and maintained through a rigorous and efficient process
- DO-254 and IEC-61508 compliance if required

Key Benefits

- No cost for hardware/tool version update/upgrade
- No time to re-generate the cores for different targets and/or tools
- Considerably faster simulations compared to vendor pre-synthesized IP Cores
- Configurable high performance VHDL modules available at no cost
- Customization available on demand
- More than 30 useful functions in the ces_math package
- More than 5.000 lines of VHDL source code and 2000 lines of comments
- CES internal VHDL coding standard to help you quickly understand the source code
- The ces_math_lib is a collection of fixed point and integer basic mathematical operations and is ideal for expert designers as well as beginners
- Ideal for Companies who start to work on FPGA design to start designing with a complete library of modules as well as expert designers.

Applications

- All FPGA\CPLD design

Deliverables

- VHDL source code
- Full set of documentation

Who we are

Campera Electronic Systems (CES) is a high technology, privately held, startup based in Livorno, Italy, with more than 10 years of experience on high performance FPGA design and Digital Signal Processing.
Established in March 2014 has grown rapidly with a focus on FPGA and its applications. The Company has developed proprietary HDL Design Flow, techniques and utilities and an immense HDL IP cores library, with fully verified high performance building blocks.

Benefits of libraries

VHDL libraries are a powerful mechanism the language offer to collect common modules together for reuse. Reuse is a key to success with FPGA design, it helps to design faster, easier and with verified and validated modules. Designing and testing a general purpose library is often considered a time consuming effort and most often there is no time for FPGA designers to build a complete general purpose library.
Using our library allow designers to focus on high-level design without wasting time to develop building blocks.

Quality and support

Campera Electronic Systems works to the highest quality standards and developed a rigorous design flow that dramatically reduce design flaws at each stage of the development process.
Customers with a valid support contract can benefit from our 24/7 support by mail and phone, all optional modules, testbenches and more.

Contacts

Via Aurelia 136, Stagno, Livorno, 57017, Italy
(+39) 0586-941403
info@campera-es.com
www.campera-es.com

CES Math Library: list of IP cores

CES MATH LIBRARY MODULES

Module name	*Description*
ces_math_add_sub	Configurable adder or subtractor for signed or unsigned numbers
ces_math_adder_tree	Configurable parallel adder for signed and unsigned numbers
ces_math_delay_complex	Delay for real and imaginary part of complex signals
ces_math_divider	Configurable divider with quotient and remainder of division
ces_math_fi_add_sub	Configurable fixed point adder or subtractor
ces_math_fi_mult	Configurable fixed point multiplier
ces_math_format	Configurable formatting for type, width, fixed point representation
ces_math_interp	Configurable interpolation module (linear interpolation supported)
ces_math_mult_add	Configurable adder of sums of multiplications for signed and unsigned
ces_math_mult_cmplx	Configurable multiplier for complex numbers
ces_math_cordic	Configurable precision module for trigonometric functions
ces_math_pkg	A great collection of essential mathematical and logical functions
ces_math_rng	Random noise generator with configurable distribution
ces_math_mean	Module to compute average (configurable window, weighting)

Each VHDL module in the Math Library can be easily configured via generics, reset type (sync or async), reset level (active low or active high), output value on reset, data width and arithmetic representation, to mention a few.
To allow for proper instantiation of hard core modules (such as Block Ram or DSP) a generic with vendor, synthesis tool and other specific information is propagated to each module.

CES MATH LIBRARY OPTIONS

Customization	Customers can add specific features or functionalities to each module on demand
Safety critical book	Verification and validation reports for safety critical applications (DO-254 and EC-61508) can be provided on demand.
AXI wrapper option	AXI4, AXI4 Stream and AXI4 Lite wrapper can be supplied on demand
VHDL 2008 version	Customers using VHDL 2008 can benefit of the readability and other improvements introduced with VHDL 2008. All the Utility modules have a corresponding VHDL 2008 version which can be supplied on demand

Library Facts Table

<table>
<tr><td>Tested on Hardware: YES</td><td>Deliverables</td><td>Supported FPGAs</td></tr>
<tr><td>Verification and Validation (opt)</td><td rowspan="6">VHDL Source Code

Documentation</td><td>Any</td></tr>
<tr><td rowspan="5">Self checking test bench

Static timing analysis

Code coverage

Linting</td><td>Supported Simulators</td></tr>
<tr><td>Active-HDL v9.1 or later and Riviera Pro v2014.02 or later</td></tr>
<tr><td>Supported Synthesizers</td></tr>
<tr><td>Mentor Precision r2013b.15 or later, Xilinx ISE 14.7/Vivado 2013.4 or later, Quartus II v.14 or later,</td></tr>
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