Simplifying FPGA Complexity

CAMPERA electronic systems

CES Code Optimization Facts

ASIP

Campera Electronic Systems has more than 10 years of FPGA HDL development experience. More than 20 high performance different design has been developed and tested on high-end FPGA devices. Our unique mixture of competencies from algorithm design up to HDL and software design guarantees that every single aspect of the Customer's design is fully analyzed and the best solution selected.
We help our Customers to improve the performance of their products without having to re-design the hardware, improving the maximum frequency for the FPGA or reducing the resource usage.

Key Features

- Proprietary optimization techniques to automatically analyze and modify the original project
- Comprehensive code review with more than 100 checklist points to reduce design flaws.
- Adherence to coding standard available on request. Through proprietary scripts the code is parsed and all items (signals, ports, generics and so on) are properly refactored to a coding standard for maximum readability, portability and future maintainability.
- Industry standard tool for Linting and code analysis (Aldec Alint with proprietary policy, customization available on demand)
- **No initial cost**: we optimize your design, you see the results and then you decide whether to move further.
- Ideal also as a external independent review of the code

Key Benefits

- Optimization of up to 20% in terms of speed, power and resource usage
- Customization available on demand
- Improve the overall quality and aspect of your source code and deliverables, no more negative feedbacks from your Customers.
- CES internal VHDL coding standard to help you quickly understand the source code
- Reducing resource usage and increasing the maximum operating frequency means you can save money and time using less expensive FPGA, or complete a design iteration in less time

Applications

- All FPGA\CPLD design
- Efficient on VHDL code, no further optimization can be made on vendor IP cores or schematic/block design

Deliverables

- Full project with source code as received from the Customer
- Full set of documentation with code quality reports

Who we are

Campera Electronic Systems (CES) is a high technology, privately held, startup based in Livorno, Italy, with more than 10 years of experience on high performance FPGA design and Digital Signal Processing.
Established in March 2014 has grown rapidly with a focus on FPGA and its applications. The Company has developed proprietary HDL Design Flow, techniques and utilities and an immense HDL IP cores library, with fully verified high performance building blocks.

How we work

Client confidentiality and privacy is as important to us as it is to our Clients.
Campera team can work both in-house and onsite at the customer's own premises for activities of a more sensitive nature.
We work to the highest quality standards and we developed a rigorous design flow that dramatically reduce design flaws at each stage of the development process.

Quality and support

Campera Electronic Systems works to the highest quality standards and developed a rigorous design flow that dramatically reduce design flaws at each stage of the development process.
Customers with a valid support contract can benefit from our 24/7 support by mail and phone, all optional modules, testbenches and more.

Contacts

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